Wavecrest's LVDS Signal Integrity Solutions

Low Voltage Differential Signaling (LVDS) is quickly becoming a popular standard for high-speed, low power data transfer for a wide variety of applications such as display graphics, inside the box busses, and other high speed, low power data transfer applications. As bus speeds have increased jitter has become a crucial parameter to characterize. As a result it has become increasingly important to characterize the jitter and other critical timing parameters of these systems and components.

Wavecrest's LVDS signal integrity solution enables designers and engineers to fully characterize and debug their components or systems. With the SIA-3000 Signal Integrity Analyzer and VISI Databus software, differential LVDS clock and data signals can be characterized for timing, clock and data jitter, clock-to-data skew, channel-to-channel skew, and Bit Error Rate (BER) on up to ten channels in parallel. The analysis can be done using one reference clock and up to nine data channels. Users can input the setup and Hold specifications and they are illustrated on the graphical user interface. Setup and Hold violations can be measured based on the actual mean of the data histogram referenced to the clock edge. Another option for determining setup and hold measurements uses the worst case data edge location. This method uses Wavecrest's patented TailFit™algorithm allowing for quick long term system reliability predictions. Figure 1 shows two views of the DataBus tool. In the top portion the mean period of the clock is displayed as a vertical line. The histograms on either side of the line display the data histograms before and after a clock cycle. The bottom portion of figure 1 shows the statistical long term BER in the form of a bathtub curve. This view is used to determine long-term system reliability. Further analysis algorithms provide total jitter separation into deterministic and random components for both the clock and data signals, allowing easy identification of signal integrity problems such as Crosstalk, EMI or bandwidth limitations.

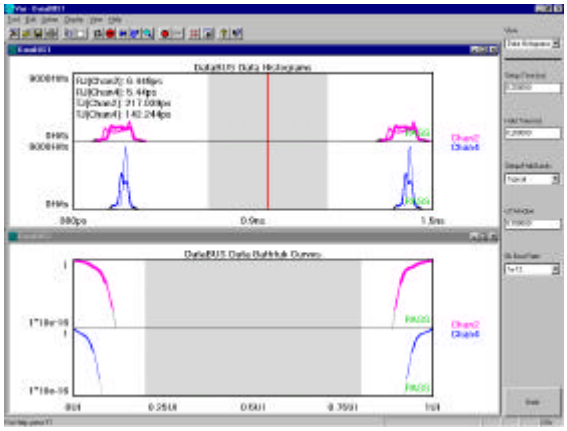

Figure 1. Setup and hold and long term BER (Bathtub Curve) views

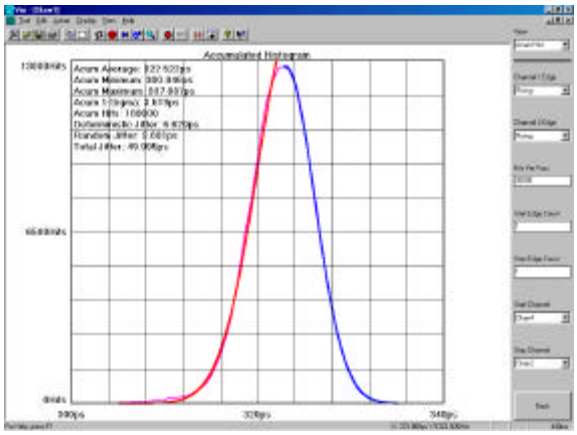

Figure 2. Propagation delay and jitter produced by an LVDS driver.

Other analysis software provides information about the signal integrity of the clock signal including complete jitter separation. Propagation delays of ICs can be measured and the amount of jitter added by the device can also be measured. For example, the mean of the histogram in figure 2 shows the propagation delay of an LVDS driver while the jitter generated by the driver is represented by the overall shape of the histogram. This allows the designer to specify how much jitter a given IC will add to an overall jitter budget. In this example, the histogram shows that the IC propagation delay is 322 ps and the IC adds 3.6 ps of RJ and 6.6 ps of DJ with a TJ of 49.9 ps at 10^{-12} BER

Wavecrest also recommends test terminations for different LVDS applications. Contact a Wavecrest applications engineer for information on what termination solution is best for your application.